This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Currently Amended) A method for lithographic process window optimization of an integrated circuit layout on a wafer and of superimposable masks and mask levels for fabrication of the integrated circuit layouts that are illuminated by beams of light radiation from a range of directions, said method comprising:

specifying a preliminary set of printed circuit feature edge locations, the model region at each edge location being recentered upon the printed edge of said circuit layout reaching the exterior of said model region;

specifying a set of linked constraints on allowable positions for the edges of said circuit features;

initially centering trust regions at the preliminary locations of said circuit feature edges;

computing models of the intensity of images projected within said trust region; and

adjusting shapes provided on said masks and intensities of said light beams illuminating the masks to project images on the wafer which satisfy the linked set of constraints over as wide a range of exposures as possible based on the computing models.

Claim 2 (Cancelled).

3. (Original) A method as claimed in Claim 1, wherein said integrated circuit features are simultaneously optimized on a plurality of mask levels through the linked involvement of a plurality of circuit feature edges.

4. (Original) A method as claimed in Claim 1, wherein said allowable positions of said edges are shiftable within a range in which the variation of image intensity at the image sidewalls is approximately linear or quadratic in nature.

5. (Original) A method as claimed in Claim 4, wherein said allowable shifts in the edges are implemented in parallel with trust region constraints on edge positions to effect said circuit layout optimization.

6. (Currently Amended) A system for lithographic process window optimization of an integrated circuit layout on a wafer and of superimposable masks and mask levels for fabrication of the integrated circuit layouts that are illuminated by beams of light radiation from a range of directions, said system comprising:

specifying a preliminary set of printed circuit feature edge locations, the model region at each edge location being recentered upon the printed edge of said circuit layout reaching the exterior of said model region;

specifying a set of linked constraints on allowable positions for the edges of said circuit features;

initially centering trust regions at the preliminary locations of said circuit feature edges;

computing models of the intensity of images projected within said trust region; and

adjusting shapes provided on said masks and intensities of said light beams illuminating the masks to project images on the wafer which satisfy the linked set of constraints over as wide a range of exposures as possible based on the computing models.

Claim 7 (Cancelled).

8. (Original) A system as claimed in Claim 6, wherein said integrated circuit features are simultaneously optimized on a plurality of mask levels through the linked involvement of a plurality of circuit feature edges.

9. (Original) A system as claimed in Claim 6, wherein said allowable positions of said edges are shiftable within a range in which the variation of image intensity at the image sidewalls is approximately linear or quadratic in nature.

10. (Original) A system as claimed in Claim 9, wherein said allowable shifts in the edges are implemented in parallel with trust region constraints on mask variables to effect said circuit layout optimization.

11. (Currently Amended) A method executed by a computer under the control of a program and a memory for storing said program for simultaneous lithographic process window optimization of an integrated circuit layout on a wafer and of superimposable masks and mask levels for fabrication of the integrated circuit layouts that are illuminated by beams of light radiation from a range of directions, said method comprising:

specifying a preliminary set of printed circuit feature edge locations, the model region at each edge location being recentered upon the printed edge of said circuit layout reaching the exterior of said model region;

specifying a set of linked constraints on allowable positions for the edges of said circuit features;

initially centering trust regions at the preliminary locations of said circuit feature edges;

computing models of the intensity of images projected within said trust region; and

adjusting shapes provided on said masks and intensities of said light beams illuminating the masks to project images on the wafer which satisfy the linked set of constraints over as wide a range of exposures as possible based on the computing models.

Claim 12 (Cancelled).

13. (Original) A method as claimed in Claim 11, wherein said integrated circuit features are simultaneously optimized on a plurality of mask levels through the linked involvement of a plurality of circuit feature edges.

14. (Original) A method as claimed in Claim 13, wherein said allowable positions of said edges are shiftable within a range in which the variation of image intensity at the image sidewalls is approximately linear or quadratic in nature.

15. (Original) A method as claimed in Claim 14, wherein said allowable shifts in the edges are implemented in parallel with trust region constraints on mask variables to effect said circuit layout optimization.